100 MHz TO 20 GHz MONOLITHIC SINGLE-POLE, TWO-, THREE-, AND FOUR-THROW GaAs PIN DIODE SWITCHES

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ABSTRACT

Monolithic GaAs PIN diode single-pole, two-, three-, and four-throw switch circuits provide low noise figure and insertion loss performance over a 2-decade + 1-octave bandwidth. From 100 MHz to 20 GHz, the measured noise figure and insertion loss for the three switch types are less than 1 dB in the through path, with greater than 45 dB of isolation in the off paths. These state-of-the-art results are obtained using a vertical PIN diode process on metallorganic chemical vapor deposition (MOCVD) material. Each of the three PIN diode switch types has been designed with and without on-chip bias networks. This paper compares the performance demonstrated by this family of six single-pole, two-, three-, and four-throw switch circuits.

INTRODUCTION

Monolithic GaAs PIN diodes have demonstrated superior performance in a number of switching and control circuits[1,2]. The low on-state resistance and low off-state capacitance of the GaAs PIN diode, coupled with the small physical size of the diode, allow circuit topologies not even possible with field effect transistor (FET)-based technology. A production process for monolithic PIN diodes has been established[3], and preliminary elevated life tests on several PIN diodes show no degradation in performance after 1,600 hours at 275°C. The unique features of the PIN diode are evident in the design and performance presented below.

DIODE MODELING

An RF model of the PIN diode is shown in Figure 1. The impedance of the PIN diode is a function of the dc current as indicated in the figure. With 0 current flow, the diode looks capacitive. As current flows through the diode, the impedance looks resistive. For typical MOCVD diodes, the RF gradient is 6 mV. This model works quite well above the diode's lower frequency limit of 80 MHz. A more complete model taking into account lower frequency operation is shown in Figure 2. The break frequency between low-frequency and high-frequency operation is determined by the storage time of the diode (~2 ns) and is represented by the 75-pF capacitor. The dc gradient is typically 45 to 52 mV.

RF DESIGN

Figure 3(A) shows a simplified schematic for the single-pole, two-throw switch without bias networks and Figure 3(B) shows how the bias networks are implemented in the switch. A series-shunt-shunt switch arm configuration was chosen to

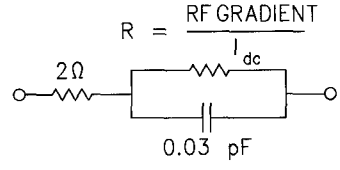

Figure 1. Simplified RF Model of PIN Diode

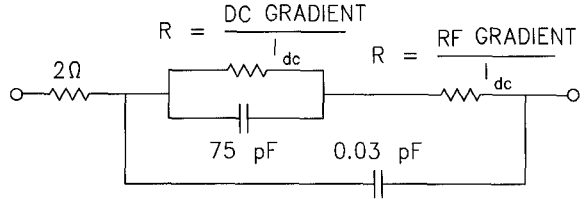

Figure 2. RF Model of PIN Diode

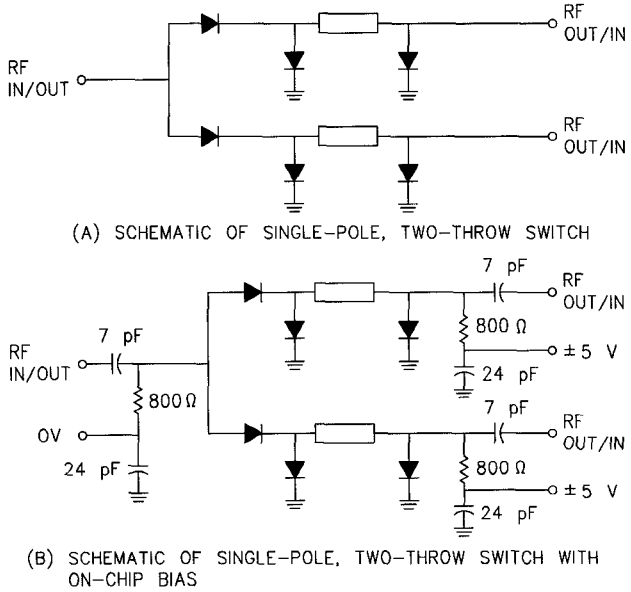

Figure 3. Single-Pole, Two-Throw Switch Schematics, With and Without Bias

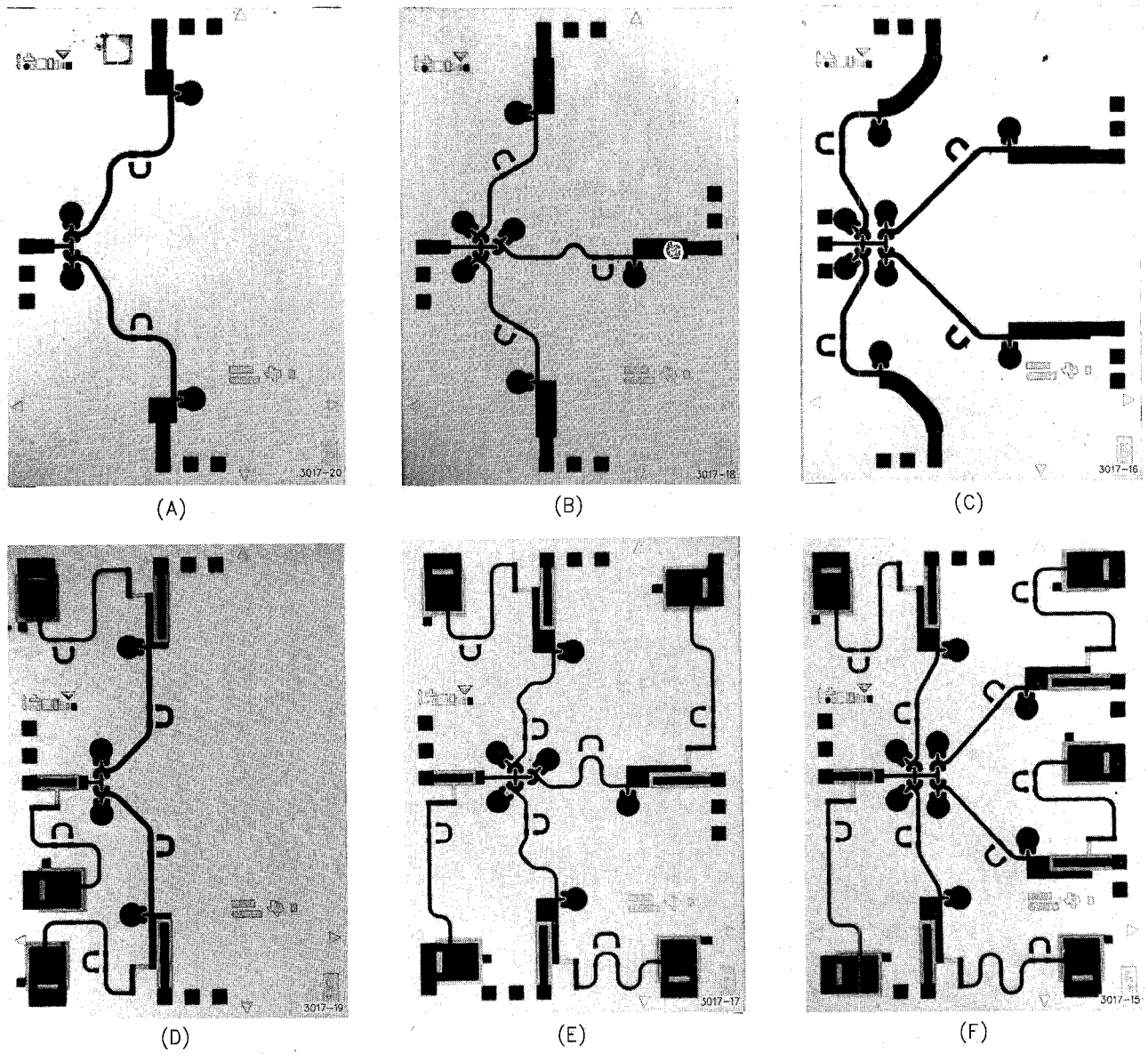

Figure 4. Single-Pole, Two-, Three-, and Four-Throw Switches

minimize the through loss, which is dominated by the series diode's on-resistance, and, at the same time, to maximize the isolation. The transmission line separating the two shunt diodes provides optimum isolation in the switch off arms at the higher frequencies of operation where the line length reaches a quarter wavelength. The width of this transmission line is also critical in matching the parasitic capacitance of the shunt diodes in the through state. The simplicity of this broadband circuit can be attributed directly to the low parasitic capacitance and resistance of the monolithic PIN diodes. The bias networks shown in Figure 3(B) are designed to operate between +5 and −5 V. A bias of −5 V on the through-path arm draws current through the series PIN diode, which is dc-grounded at the input, while reverse-biasing the shunt diodes. A +5 V bias on the off arms reverse-biases the series PIN diode while forward-biasing the shunt diodes on. The 800 Ω resistance value in each arm of the bias network was selected to provide a 2 mA current flow in each diode. The quarter-wave transmission line in series with the shunt resistor minimizes the insertion loss associated with the bias network at the upper frequency band. The insertion loss of the switch arm is dominated by the bias circuit and not by the series diode. Measurements show that the switch insertion loss is lower with a 2 mA series diode bias and 800 Ω bias resistors than designs with a 4 mA series diode bias and 400 Ω bias resistors. Designs for operation from a ±10 or ±12 V power supply would allow larger bias resistors and lower the insertion loss of each switch arm.

RF PERFORMANCE

Figure 4(A–F) shows photographs of the six monolithic switch circuits. The chip sizes are identical so as to fit easily onto a single mask set and are determined by the size of the single-pole, four-throw switch with on-chip bias. The chip

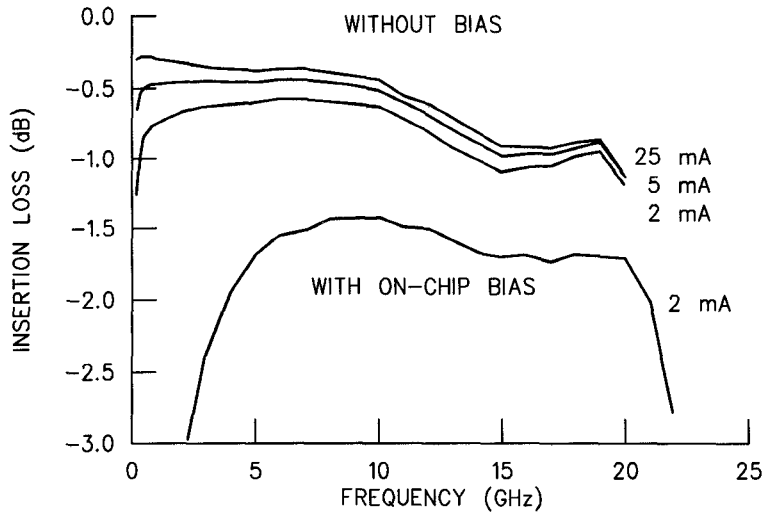

Figure 5. Single-Pole-Two-Throw Switch Insertion Loss Performance

sizes are 100 × 140 × 4 mils. Figures 5 and 6 show the insertion loss of the single-pole, two-throw and single-pole, four-throw switches, both with and without bias networks and blocking capacitors. The performance of the switch without on-chip bias networks is measured with bias Ts and is shown as a function of the current in the series PIN diode. The current in the off arms is 2 mA per arm. The performance of the switch with on-chip bias networks is measured with the ±5 V supply. The current in both the on and off arms is 2 mA. Figures 7 and 8 show the isolation of the single-pole, two-throw and single pole, four-throw switches with and without on-chip bias networks and blocking capacitors. From Figures 5 and 6, it is evident that the bandwidth of the switches with blocking capacitors and on-chip bias has been constricted to the 4 GHz to 20 GHz band. The loss also has increased from 1 dB to 1.75 dB. The rolloff at 4 GHz in the switches with on-chip bias is caused primarily by the 7 pF input and output blocking capacitors. The additional 0.75 dB of insertion loss is due to the 800 Ω shunt bias resistors. The difference in insertion loss between the two-throw and four-throw switches is about 0.2 dB through 19.5 GHz, where the loss of the four-throw begins to roll off. The insertion loss of the two-throw switch does not begin to roll off until 20.5 GHz. The isolation is greater than 42 dB across the band. Table 1 summarizes the RF performance of all six switch types. The noise figure has been measured from 20 MHz to 18 GHz, and no excess noise has been measured. The only contribution to the noise figure is the insertion loss of the switch. The 1-dB gain compression for the switches without on-chip bias is 21 dBm. For the switches with on-chip bias, the 1-dB gain compression is 26 dBm for ±5 V operation and 30 dBm for ±10 V operation. The power handling capability of the switches could be improved by RF-grounding all the shunt diodes through capacitors and then reverse-biasing the shunt diodes in the through path. The turn-on/off time for the switches without bias networks is 15 ns.

The return loss of the single-pole, two-throw switch without bias is greater than 20 dB through 11 GHz and greater than 15 dB through 19 GHz. The return loss of the single-pole, four-throw switch without bias is greater than 20 dB through 8.6 GHz and greater than 15 dB through 19 GHz.

TABLE 1. PERFORMANCE SUMMARY FOR SIX MONOLITHIC SWITCH CIRCUITS

Switch Type	Frequency Band (GHz)	Insertion Loss (dB)	Isolation (dB)
Two-throw with bias	0.1–20	1.0	42
Three-throw with bias	0.1–20	1.1	42
Four-throw with bias	0.1–20	1.2	42
Two-throw without bias	4.0–20	1.8	42
Three-throw without bias	4.0–20	2.0	42
Four-throw without bias	4.0–20	2.1	42

CONCLUSIONS

A family of low-loss, low-noise figure, high-isolation PIN diode switches have demonstrated broadband performance needed for many applications. The key to this exceptional performance is the low on-resistance and minimal off-capacitance of the monolithic MOCVD-grown PIN diode.

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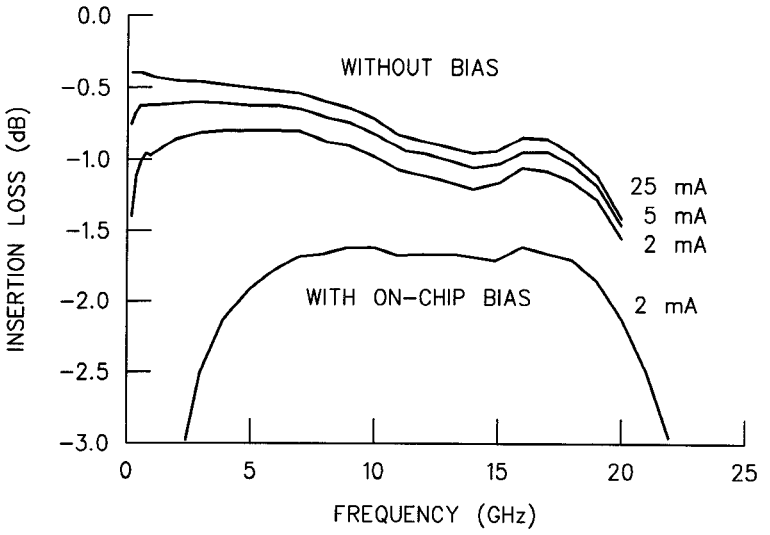

Figure 6. Single-Pole, Four-Throw Switch Insertion Loss Performance

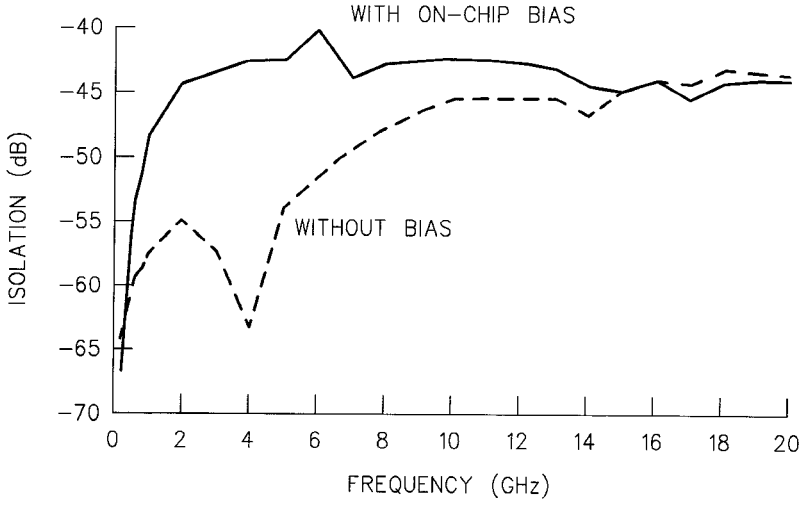

Figure 7. Single-Pole, Two-Throw Switch Isolation Performance

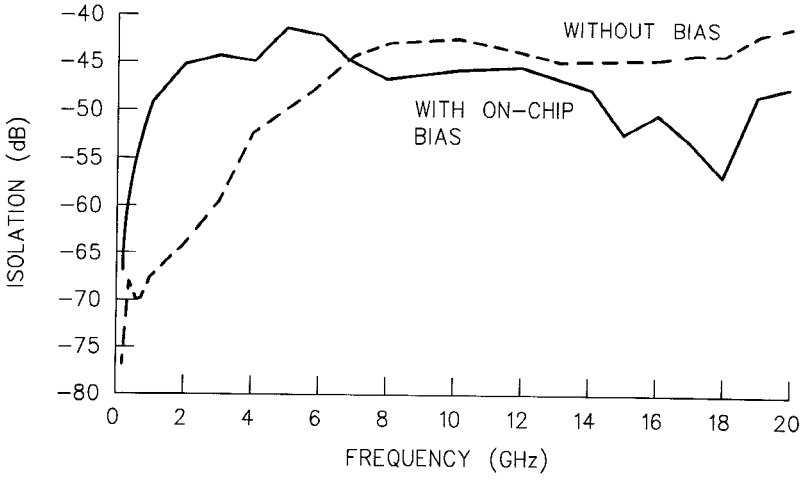

Figure 8. Single-Pole, Four-Throw Switch Isolation Performance